EXHIBIT B

ID696794– ID abstract

The invention relates to a method for handling a failing clock in an electronic system.

Conventionally, in synchronous electronic systems, a failing clock is detected by means of a watchdog timer, which generates a reset for the micro controller in the absence of a clock signal.

Figure A. shows the synchronous failsafe principle. In normal operation mode the Watch Dog Timer (WDT) will be triggered regular, in case this triggering stops the WDT output will become active (after a defined period) and will reset the microcontroller So this extra hardware is needed to 'execute' a failsafe event, for example a reset to turn off outputs and to reset the microcontroller.

In a system comprising an asynchronous micro controller it is not possible to use such a watch dog timer.

By making use of asynchronous technology, whereby the clock generation circuit is not necessary for the execution of the microcontrollers instructions, extra hardware can be avoided to enter this failsafe event and this saves costs, refer to figure B.

In this case however a special clock source is necessary with a status output, which shows the status if the oscillator is running. By connecting this output to for example to an interrupt request input of the microcontroller, the microcontroller can detect the error condition. This event will start a special software routine, which handles code related to a failing clock source without the need of the clock source.

So the advantage of this solution is: a dedicated software routine can be started to execute dedicated code and also having to possibility to modify this code.